ABSTRACT

Variations in memory array and cell configuration are shown, which eliminate punch-through disturb, reverse-tunnel. Several configurations are shown which range from combined and separate source lines for each row of cells, a two transistor cell containing a read transistor and a program transistor connected by a merged floating gate, and a two transistor cell where the program transistor has an extra implant to raise the Vt of the transistor to protect against punch-through disturb. A method is also described to rewrite disturbed cells, which were not selected to be programmed. .